What Is Claimed Is:

1. A logic system with adaptive supply voltage control, comprising:

a logic circuit clocked by a clock signal of a predetermined frequency generated by a clock generating circuit, said logic circuit having a critical path delay being equal to or shorter than a period of the clock signal; and

a voltage conversion circuit for dynamically regulating a supply voltage for powering said logic circuit based on a bias voltage of the clock generating circuit.

2. The logic system with adaptive supply voltage control of claim 1, wherein the clock generating circuit comprises an oscillator and wherein the period of the clock signal is equal to two times of a loop delay of the oscillator.

3. The logic system with adaptive supply voltage control of claim 1, wherein the clock generating circuit comprises an oscillator and a divide-by-k divider connected at the output of the oscillator, and wherein the period of the clock signal is equal to 2 times of a loop delay of the oscillator times k.

4. The logic system with adaptive supply voltage control of claim 1, wherein the period of the clock signal is longer than said critical path delay of said logic circuit.

5. The logic system with adaptive supply voltage control of claim 1, wherein the supply voltage for powering said logic circuit is dynamically regulated such that said

critical path delay of said logic circuit approximately matches the period of the clock signal.

6. The logic system with adaptive supply voltage control of claim 1, wherein said voltage conversion circuit comprises a voltage regulator.

7. The logic system with adaptive supply voltage control of claim 1, wherein said voltage conversion circuit comprises a DC-DC converter.

8. The logic system with adaptive supply voltage control of claim 1, wherein a delay matching circuit is employed to achieve matching between said critical path delay of said logic circuit and the period of the clock signal.

9. The logic system with adaptive supply voltage control of claim 1, wherein a DLL (delay-locked loop) circuit is employed to achieve matching between said critical path delay of said logic circuit and the period of the clock signal.

10. A logic system with adaptive supply voltage control, comprising:

a logic circuit having a power supply terminal for receiving a supply voltage and a clock input terminal for receiving a clock signal of a predetermined frequency from a clock generating circuit, said logic circuit having similar delay characteristics with the clock generating circuit; and

a voltage conversion circuit for dynamically regulating the supply voltage at said power supply terminal of said logic circuit on the basis of a bias voltage of the clock

generating circuit.

11. The logic system with adaptive supply voltage control of claim 10, wherein the clock generating circuit comprises an oscillator and wherein a period of the clock signal is equal to two times of a loop delay of the oscillator.

12. The logic system with adaptive supply voltage control of claim 10, wherein the clock generating circuit comprises an oscillator and a divide-by-k divider connected at the output of the oscillator, and wherein a period of the clock generating circuit is equal to two times of a loop delay of the oscillator times k.

13. The logic system with adaptive supply voltage control of claim 10, wherein a period of the clock signal is slightly longer than a critical path delay of said logic circuit.

14. The logic system with adaptive supply voltage control of claim 10, wherein the regulated supply voltage at said power supply terminal of said logic circuit is higher than the bias voltage of the clock generating circuit.

15. The logic system with adaptive supply voltage control of claim 10, wherein the regulated supply voltage at said power supply terminal of said logic circuit is equal to the bias voltage of the clock generating circuit.

16. The logic system with adaptive supply voltage control of claim 10, wherein said voltage conversion circuit comprises a voltage regulator.

17. The logic system with adaptive supply voltage control of claim 10, wherein said voltage conversion circuit comprises a DC-DC converter.

18. The logic system with adaptive supply voltage control of claim 10, wherein logic elements constituting said logic circuit have similar delay sensitivity to supply voltage, temperature and process shifts with delay elements in the clock generating circuit.

19. An adaptive supply voltage control method for a logic circuit clocked by a clock signal of a predetermined frequency from a clock generating circuit, said logic circuit having a critical path delay being equal to or shorter than a period of the clock signal, said method comprising dynamically regulating a supply voltage for powering said logic circuit based on a bias voltage of the clock generating circuit.

20. The adaptive supply voltage control method of claim 19, wherein the supply voltage for powering said logic circuit is dynamically regulated such that said critical path delay of said logic circuit approximately matches the period of the clock signal.

21. An adaptive supply voltage control method for a logic circuit clocked by a clock signal of a predetermined frequency from a clock generating circuit, said logic circuit having similar delay characteristics with the clock generating circuit, said method comprising dynamically regulating a supply voltage for said logic circuit on the basis of a bias voltage of the clock generating circuit.

22. The adaptive supply voltage control method of claim 21, wherein a period of the clock signal is longer than a critical path delay of said logic circuit.

23. The adaptive supply voltage control method of claim 21, wherein the regulated supply voltage for said logic circuit is equal to or higher than the bias voltage of the clock generating circuit.